Atty. Dkt. No. 200312670-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Meyer et al. Title: BONDING AN INTERCONNECT TO A CIRCUIT DEVICE AND RELATED DEVICES Appl. No.: 10/822,064 Filing Date: 04/08/2004 Examiner: Chang, Rick Kiltae Art Unit: 3726	**CERTIFICATE OF FACSIMILE TRANSMISSION** I hereby certify that this paper is being facsimile transmitted to the **United States Patent and Trademark Office, Alexandria, Virginia** on the date below. *Todd A. Rathe* (Printed Name) (Signature) (Date of Deposit)

BRIEF ON APPEAL

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. **Real Party in Interest**

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, California. The general or managing partner of HPDC is HPQ Holdings, LLC.

2. Related Appeals and Interferences

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the present appeal, that are known to Appellants or Appellants' patent representative.

3. Status of Claims

Claims 10, 11, 30 and 40 are presently withdrawn from consideration; claims 29 and 88-93 are presently objected to; and claims 1-9, 12-19, 21, 25-28, 31-39, 41-48 and 87 are presently rejected. The present appeal is directed to claims 1-9, 12-19, 21, 25-29, 31-39, 31-39, 41-48 and 87-93, i.e., all of the presently pending claims that stand rejected in this application.

4. Status of Amendments

No amendments were filed after the Final Office Action dated February 23, 2009.

5. Summary of Claimed Subject Matter

A. Claim 1

Claim 1 recites a method comprising:

orienting an interconnect with respect to a dense circuit device (page 8, lines 11-12);

pressing the interconnect to the dense circuit device using a substrate (page 12, lines 18-30); and

bonding the substrate to the dense circuit device sufficient to maintain the interconnect against the dense circuit device(page 12, lines 18-30),

wherein the act of pressing comprises mechanically clamping the interconnect between the dense circuit device and the substrate (page 12, lines 18-30; page 13, lines 4-23; page 15, lines 2-4).

B. Claim 2

Claim 2 depends from claim 1 and recites that the act of orienting the interconnect comprises fitting a negative in the interconnect over a projection on the dense circuit device such that the negative receives and at least partially surrounds the projection. (Page 9, lines 26-30)

C. Claim 3

Claim 3 depends from claim 1 and recites that the act of orienting comprises orienting wires of the interconnect with electrical bond pads of the dense circuit device. (page 8, lines 11-12)

D. Claim 4

Claim 4 depends from claim 3 and further recites that the wires and the electrical bond pads overlap and at the overlap have a breadth from tens of nanometers to tens of microns (page 18, lines 14-16).

E. Claim 5

Claim 5 depends from claim 3 and further recites that the wires and the electrical bond pads overlap and at the overlap have a space from tens of nanometers to tens of microns (page 18, lines 14-16).

F. Claim 6

Claim 6 depends from claim 3 and further recites that the wires and the electrical bond pads overlap and at the overlap have a breadth of less than one micron (page 18, lines 21-22).

G. Claim 7

Claim 7 depends from claim 3 and further recites that the wires and the electrical bond pads overlap and at the overlap have a space of less than one micron (page 18, lines 21-22).

H. Claim 9

Claim 9 depends from page claim 1 and further recites that the act of bonding comprises covalently bonding the dense circuit device to the substrate. (page 12, lines 18-30; page 13, lines 4-23; page 15, lines 2-4)

I. Claim 12

Claim 12 depends from claim 1 further recites that the act of bonding is performed at low temperature. (Page 11, lines 29-30; page 12, lines 30-32)

J. Claim 13

Claim 13 depends from claim 12 and further recites that the low temperature comprises room temperature. (Page 11, lines 29-30; page 12, lines 30-32)

K. Claim 14

Claim 14 depends from claim 1 and further recites:

covalently bonding wires of the interconnect with electrical bond pads of the dense circuit device. (Page 12, lines 18-29)

L. Claim 15

Claim 15 depends from claim 1 further recites that the dense circuit device comprises a length or width of less than or about twenty-five millimeters. (page 19, lines 17-18)

M. Claim 25

Claim 25 recites a method comprising:

providing a dense circuit device having a first surface prepared for covalent bonding; (page 7, lines 8-11)

providing a substrate having a second surface prepared for covalent bonding; (page 7, lines 8-11)

orienting an interconnect between the dense circuit device and the substrate; (page 8, lines 11-12) and

mechanically clamping the interconnect between the dense circuit device and the substrate by covalently bonding the first surface to the second surface.

N. Claim 28

Claim 28 depends from claim 25 and further recites that the dense circuit device comprises a projection comprising the first surface and the act of orienting comprises fitting a negative in the interconnect over the projection such that the negative receives and at least partially surrounds the projection. (Page 9, lines 26-30)

O. Claim 29

Claim 29 depends from claim 25 and further recites that the substrate comprises a projection comprising the second surface and the act of orienting comprises fitting a negative in the interconnect over the projection such that the negative receives and at least partially surrounds the projection. (Page 9, lines 26-30)

P. Claim 31

Claim 31 depends from claim 25 and further recites that the act of orienting comprises orienting wires of the interconnect with electrical bond pads of the dense circuit device. (page 8, lines 11-12).

Q. Claim 32

Claim 32 depends from claim 31 and further recites that the wires and the electrical bond pads overlap and at the overlap have a breadth from about tens of nanometers to tens of microns. (page 18, lines 14-16)..

R. Claim 33

Claim 33 depends from claim 31 and further recites that the wires and the electrical bond pads overlap and at the overlap have a breadth of less than one micron. (page 18, lines 21-22).

S. Claim 35

Claim 35 depends from claim 25 and further recites that the act of mechanically clamping is performed at low temperature. (Page 11, lines 29-30; page 12, lines 30-32)

T. Claim 36

Claim 36 depends from claim 35 and further recites that the low temperature comprises room temperature. . (Page 11, lines 29-30; page 12, lines 30-32)

U. Claim 37

Claim 37 depends from claim 25 and further recites forming a compliant layer between the interconnect and the substrate. (Page 8, lines 21-26)

V. Claim 38

Claim 38 depends from claim 25 and further recites that the interconnect includes wires and a compliant layer. (Page 8, lines 11-26)

W. Claim 39

Claim 39 depends from claim 25 and recites that the interconnect includes wires, a compliant layer, and a stiffening layer. (Page 16, lines 7-9)

X. Claim 43

Claim 43 depends from claim 42 which recites that the substrate comprises a second dense circuit device. Claim 43 further recites that the substrate and the first dense circuit device are separated by a spacer having conductive vias enabling electrical communication between the second dense circuit device and the first dense circuit device. (Page 14, lines 17-21)

Y. Claim 44

Claim 44 recites a method comprising:

planarizing a first surface of a dense circuit device; (page 6, lines 25-28)

planarizing a second surface of a spacer substrate; (page 7, lines 11-14

planarizing a third surface of the spacer substrate; (page 7, lines 25-28)

planarizing a fourth surface of a clamping substrate; (page 11, lines 1-5)

covalently bonding one of the (a) first surface to the second surface or (b) the third surface to the fourth surface; (page 12, lines 18-30; page 13, lines 4-23; page 15, lines 2-4)

orienting an interconnect between the dense circuit device and the clamping substrate; (page 8, lines 11-12) and

mechanically clamping the interconnect to the dense circuit device by covalently bonding an other of the (a) first surface to the second surface or (b) the third surface to the fourth surface. (page 12, lines 18-30; page 13, lines 4-23; page 15, lines 2-4)

Z. Claim 46

Claim 46 depends from claim 44 and further recites that the dense circuit device comprises a dimension of less than or about twenty-five millimeters. (page 19, lines 17-18)

AA. Claim 48

Claim 48 depends from claim 47 which recites that the clamping substrate comprises a second dense circuit device. Claim 48 further recites that the interconnect comprises two sets of wires, the first set contacting the first dense circuit device and the second set contacting the second dense circuit device. (Page 24, lines 6-9)

6. Grounds of rejection to be reviewed on appeal. A concise statement of each ground of rejection presented for review.

The issues on appeal are **(1)** whether the Examiner erred in rejecting Claims 1-7 and 15-17 under 35 U.S.C. § 102(e)as being anticipated by U.S. Patent 6555908 (Eichelberger) **(2)** whether the Examiner erred in rejecting claim 8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6555908 (Eichelberger) in view of

Official Notice; and **(3)** whether the Examiner erred in rejecting claims 9, 12-14, 25-29, 31-39, 41-48 and 87 under 35 U.S.C. § 103(a) as being unpatentable over by U.S. Patent 6555908 (Eichelberger) in view of U.S. Patent 6962835 (Tong).

7. Argument

I. Legal Standards

A. Law of Anticipation

Claims 1-7 and 15-17 have been rejected under 35 U.S.C. § 102(e), which states:

> A person shall be entitled to a patent unless –
>
> ...
>
> (e) the invention was described in - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent....
>
> ....

Under Section 102, a claim is anticipated, i.e., rendered not novel, when a prior art reference discloses every limitation of the claim. In re Schreiber, 128 F.3rd 1473, 1477 (Fed. Cir.1997 "Rejections under 35 U.S.C. § 102(a) are proper only when the claimed subject matter is identically disclosed or described in the prior art." In re Arklely, Eardley, and Long, 172 U.S.P.Q. 524, 526 (CCPA 1972).

The scope of a claim in a patent application is not solely on the basis of the claim language itself, but is based upon the broadest reasonable construction of the claim in light of the specification as it would be interpreted by one of ordinary skill in the art. Phillips v. AWH Corp., 415 F.3d 1303, 1316 (Fed. Cir. 2005). The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. Id. at 1313. The specification is the single best

guide to the meaning of a disputed term in that the specification acts as a dictionary by expressly defining terms used in the claims or by defining terms by implication. Id. at 1321. A claim term may be redefined without any express statement of redefinition in the specification. Id. at 1321; Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1268 (Fed. Cir. 2001). A general usage dictionary cannot overcome art specific evidence as to the meaning of a claim term. Phillips at 1322.

B. Law of Obviousness

Claims 8, 9, 12-14, 25-29, 31-39, 41-48 and 87 are rejected under 35 U.S.C. § 103(a), which states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The legal standards under 35 U.S.C. § 103(a) are well-settled. Obviousness under 35 U.S.C. § 103(a) involves four factual inquires: 1) the scope and content of the prior art; 2) the differences between the claims and the prior art; 3) the level of ordinary skill in the pertinent art; and 4) secondary considerations, if any, of nonobviousness. See Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). "[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the

references." In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 U.S.P.Q. 2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." In re Lee, 277 F.3d 1338, 61 U.S.P.Q. 2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q. 2d 1438 (Fed. Cir. 1991). The test for determining the obviousness of combining known elements is not rigid, but depends on such factors as the interrelated teaching of multiple patents, the effects of demands known to the design community or present in the marketplace and the background knowledge possessed by a person of ordinary skill in the art. KSR Intl v. Teleflex Inc., 550 US 398, (2007). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 U.S.P.Q. 2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 312-13 (Fed. Cir. 1983)). Teaching away from the claimed invention is a strong indication of non-obviousness and an improper combination of references. U.S. v. Adams, 383 U.S. 39 (1966).

II. The Examiner's Rejection of Claims 1-7 and 15-17 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6555908 (Eichelberger) Should Be Reversed Because Eichelberger Does Not Disclose Every Limitation of Each of the Claims.

The claimed invention is not anticipated under § 102 unless each and every element of the claimed invention is found in the prior art. (Hydratech, Inc. v. Monochronal Antibodies, Inc., Fed. Cir. 1986). Accordingly, the rejection of these claims under 35 U.S.C. § 102(b) is improper and should be reversed.

A. Claim 1

Claim 1 recites a method which includes pressing an interconnect to a dense circuit device using a substrate, wherein the act of compressing comprises mechanically clamping the interconnect between the dense circuit device and the substrate.

Eichelberger fails to disclose pressing an interconnect to a dense circuit device using a substrate by mechanically clamping the interconnect between the dense circuit device and the substrate. In contrast, Eichelberger merely discloses a multi-layer polymer bump module 1000 which is soldered to a printed circuit board 1300.

In rejecting claim 1, each of claims 1-7 and 15-17 based upon Eichelberger, the Examiner simply provides an annotated copy of the disclosure of Eichelberger. In order to reject the claims, the Examiner attempts to characterize some of the layers of the unitary multilayer module 800 as the recited interconnect and other layers of the unitary multilayer module 800 as the dense circuit device.

However, this characterization is improper. Although an examiner may be allowed to apply the broadest reasonable interpretation to a claim, this characterization amounts to a distortion of the English language. Claim 1 recites that the interconnect is "pressed to the dense circuit device." One of ordinary skill in the art would never consider layers which are formed upon one another as being "pressed" towards one another.

More importantly, claim 1 recites that the interconnect is "mechanically clamped between the dense circuit device and the substrate." The definition of the verb clamp is "to fasten with or fix in a clamp". Random House College dictionary (1984). The definition of a clamp is;

> 1. A device for strengthening or supporting objects or fastening them together. 2. An appliance with opposite parts that may be brought closer together to hold or compress something.

(Random House College dictionary (1984)).

One of ordinary skill in the art would never consider an underlying layer of a multi-layer structure as being "mechanically clamped" between an overlying layer of the multilayer structure and another structure. The Examiner's argument is analogous arguing that the jelly layer of a peanut butter and jelly sandwich is "mechanically clamped" between the peanut butter and the bread. This characterization fails to hold water. Accordingly, rejection of claim 1 should be reversed. The rejection of claims 2-7 and 15-17, which depend from claim 1, should be reversed for at least the same reasons.

B. Claim 2

Claim 2 depends from claim 1. Claim 2, as amended, recites fitting a negative in the interconnect over a projection on the dense circuit device such the negative receives and at least partially surrounds the projection. Support for this amendment may be found in at least Figure 12.

Eichelberger fails to disclose fitting a negative in an interconnect over a projection on the dense circuit device such that the negative receives at least partially surrounds a projection. In the annotated Figure 13C of Eichelberger provided by the Examiner, the Examiner refers to two layers of the multilayer module 800 as the alleged projection and negative. It is clear that the alleged negative pointed to in the Figure 13C by the Examiner does not receive and at least partially surround the alleged projection pointed to in the Figure 13C by the Examiner. Accordingly, claim 2, as amended, overcomes the rejection based upon Eichelberger.

C. Claim 3

Claim 3 depends from claim 1 and recites that the active orienting comprises orienting WIRES of the interconnect with the electrical bond pads of the dense circuit device.

Eichelberger fails to disclose any wires. In contrast, Eichelberger merely discloses electrically conductive layers of a multilayer module 800. A wire is defined as "a slender, stringlike piece or filament of metal." (Random House College dictionary (1984)). An electrically conductive layer or electrically conductive traces is not a wire. One of ordinary skill in the art would not consider an electrically conductive layer of a multilayer structure to be a "wire." Accordingly, the rejection of claim 3 should be reversed. The rejection of claims 4-8 which depend from claim 3 should be reversed for at least the same additional reasons.

D. Claims 4-7 and 15

Claims 4-7 depend from claim 3 and recite various ranges of dimensions with respect to the overlap of the wires end of the electrical bond pads. Claim 15 depends from claim 1 and recites that the dense circuit device has a length a width of less than or about 25 mm. As noted in the present application, one of the problems being solved by the present method is the usual difficulty of forming interconnections when dense circuit devices and the electrical bond pads become small. (See Paragraph [0003]). Appellants' method addresses the noted problem, potentially enabling these more compact or smaller arrangement of devices to be achieved.

Eichelberger fails to disclose the recited dimensions for the overlap between the electrical bond pads and wires. Eichelberger fails to disclose the recited in dimensions for the dense circuit device. Appellants respectfully note that anticipation requires a reference to disclose each and every claimed element. Nowhere does Eichelberger even remotely mention any ranges of dimensions for such overlap or the dense circuit device. As a result, such claims cannot be anticipated by Eichelberger.

In rejecting claims 4-7, the Examiner points to structures in the annotated Figure 13C of Eichelberger with the notation "not drawn to scale." This does not establish a prima facie case of anticipation with regard to a claimed dimension. If such were the case, nearly every patent claim reciting a dimension would be invalid. The rejection of claims 4-7 as being anticipated by Eichelberger is improper and should be reversed.

III. The Examiner's Rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6555908 (Eichelberger) in view of Official Notice Should be Reversed Because It Would Not Be Obvious to Modify Eichelberger so As to Include Every Limitation of Each of the Claims.

Claim 8 depends from claim 3 and overcomes the rejection for the same reasons discussed above with respect to the rejection of claim 3 based upon Eichelberger alone.

IV. The Examiner's Rejection of Claims 9, 12-14, 25-29, 31-39, 41-48 and 87 under 35 U.S.C. § 103(a) as being unpatentable over by U.S. Patent 6555908 (Eichelberger) in view of U.S. Patent 6962835 (Tong) Should be Reversed Because It Would Not Be Obvious to Modify Eichelberger based upon Tong so As to Include Every Limitation of Each of the Claims.

A. Claims 9 and 12-13

Claims 9 and 12-13 depend from claim 1 and overcome the rejection for the same reasons discussed above with respect to the rejection of claim 1 based upon Eichelberger alone. Tong fails to satisfy the deficiencies of Eichelberger.

Moreover, claim 1, from which claims 9 and 12-14 depend, additionally recites that the substrate is bonded to the dense circuit device. Claim 9 recites that this bonding is covalent bonding. Claim 12 recites that this bonding is performed at low temperature. Claim 13 recites that this bonding is performed at room temperature.

Neither Eichelberger nor Tong, alone or in combination, disclose the use of covalent bonding, bonding at a low temperature or bonding at room temperature of a substrate to a dense circuit device. Although it may be true that Tong broadly discloses covalent bonding. Tong does not disclose covalent bonding of a substrate to a dense circuit device with an interconnect also located between the dense circuit device and the substrate.

Even assuming, arguendo, that it would be obvious to modify Eichelberger based on Tong to use a covalent bonding taught by Tong, the resulting hypothetical combination would still not result in a method in which the dense circuit device of Eichelberger would be covalent bonded, bonding at low temperature or bonding at room temperature to the substrate. At most, the resulting hypothetical combination would simply involve covalently bonding what the Examiner characterizes as the interconnect to what the Examiner characterizes as the substrate. Accordingly, the rejection of claims 9 and 12-13 should be reversed for at least this additional reason.

B. Claim 14

Claim 14 depends from claim number one and recites covalently bonding wires of the interconnect with electrical bond pads of the dense circuit device.

Once again, Eichelberger does not disclose any wires. Likewise, Tong does not disclose any wires. Accordingly, the rejection of claim 14 should be reversed.

C. Claim 25

Claim 25 recites a method which includes providing a dense circuit device having a first surface, a substrate having a second surface and mechanically clamping an interconnect between the dense circuit device and the substrate by covalently bonding the first surface and the second surface.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest a method (1) wherein a surface of a dense circuit device is covalently bonded to surface of a substrate or (2) wherein an interconnect is mechanically clamped between the dense circuit device and the substrate.

First, nowhere does Eichelberger even remotely suggest that the upper layers of the multilayer module 800 that have been characterized by the Examiner as the "dense circuit device" have a surface that is bonded to printed circuit board 1300 (characterized by the Examiner as the "substrate"). Nowhere does Eichelberger even remotely suggest that such bonding would be reform by covalent bonding. In contrast, the portion of the multilayer module 800 of Eichelberger characterized as the dense circuit device never even comes close to touching circuit board 1300.

Second, nowhere does Eichelberger or Tong even remotely suggest an interconnect that is mechanically clamped between the dense circuit device and the substrate. As noted above with respect to the rejection of claim 1 based upon Eichelberger, one of ordinary skill in the art would never consider an underlying layer of a multilayer structure to be mechanically clamped with respect to an overlying layer of a multilayer structure. Accordingly, the rejection of claim 25 should be reversed. The rejection of claims 26-29 and 31-39 and 41 43 which depend from claim 25 should be reversed for at least the same reasons.

D. Claims 28 and 29

Claim 28 and 29 depends from claim 25. Claims 2829, as amended, recite fitting a negative in the interconnect over a projection such that the negative receives the projection and at least partially surrounds a projection.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest fitting a negative in an interconnect over a projection such that the negative receives at least partially surrounds a projection. In the annotated Figure 13C of Eichelberger provided by the Examiner, the Examiner refers to two layers of the multilayer module 800 as the alleged projection and negative. It is clear that the alleged negative pointed to in the Figure 13C by the Examiner does not receive and at least partially surround the alleged projection 22 in the Figure 13C by the Examiner. Accordingly, claim 28 and 29, as amended, overcome the rejection based upon Eichelberger and Tong.

E. Claim 31

Claim 31 depends from claim 25 and recites that the active orienting comprises orienting wires of the interconnect with electoral bond pads of the dense circuit device.

Neither Eichelberger nor Tong, alone or in combination, disclose orienting wires of an interconnect with electoral bond pads of a dense circuit device. As noted above, Eichelberger does not disclose any wires. Moreover, the electrically conductive layers of the multilayer module 800 which happen to be adjacent to other electrically conductive layers of the multilayer module 800 does not constitute orienting wires with electrical bond pads. Accordingly, the rejection of claim 31 should be reversed for at least this additional reason.

F. Claim 32-33

Claims 32 and 33 depend from claim 31 and further recite a range of dimensions in which the wires and the bond pads overlap one another. As noted in the present application, one of the problems being solved by the present method is the usual difficulty of forming interconnections when dense circuit devices and the electrical bond pads become small. (See Paragraph [0003]). Appellants' method addresses the noted problem, potentially enabling these more compact or smaller arrangement of devices to be achieved.

Neither Eichelberger nor Tong disclose the recited dimensions for the overlap between the electrical bond pads and wires. Accordingly, their combination does not disclose the recited dimensions.

In rejecting claims 32 and 33, the Examiner points to structures in the annotated Figure 13C of Eichelberger with the notation "not drawn to scale." This does not establish a prima facie case of obviousness with regard to a claim dimension. If such were the case, nearly every patent claim reciting a dimension would be invalid. The rejection of claims 32 and 33 based upon Eichelberger and Tong is improper and should be reversed.

G. Claims 35-36

Moreover, claim 25, from which claims 35 and 36 depend, additionally recites that the substrate has a surface that is bonded to a surface of the dense circuit device. Claim 35 recites that this bonding is performed at low temperature. Claim 36 recites that this bonding is performed at room temperature.

Neither Eichelberger nor Tong, alone or in combination, disclose bonding at a low temperature or bonding at room temperature of a surface of a substrate to a surface of a dense circuit device. Although it may be true that Tong broadly discloses covalent bonding. Tong does not disclose covalent bonding of a substrate to a dense circuit device with an interconnect also located between the dense circuit device and the substrate.

Even assuming, arguendo, there would be obvious to modify Eichelberger based on Tong to use a covalent bonding taught by Tong, the resulting hypothetical combination would still not result in a method in which the dense circuit device of Eichelberger would be bonded at low temperature or bonded at room temperature to the substrate. At most, the resulting hypothetical combination would simply involve covalently bonding what the Examiner characterizes as the interconnect to what the Examiner characterizes as the substrate. Accordingly, the rejection of claims 35 and 36 should be reversed for at least this additional reason.

H. Claim 37

Claim 37 depends from claim 25 and recites formation client layer between the interconnect and the substrate.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest forming a compliant layer between the interconnect in the substrate. In rejecting claim 37, the Examiner refers to its annotated Figure 13C and attempts to characterize a layer of circuit board 1300 as the claimed "compliant layer." First, nowhere does Eichelberger disclose that the portion pointed to by the Examiner is compliant. Second, this portion of circuit board 1300 characterized by the Examiner as the "compliant layer" is NOT between circuit board 1300 (characterized as a substrate) and those portions of multilayer module 800 (characterized by the Examiner as the interconnect). Rather, it is actually part of circuit board 1300.

Accordingly, the rejection of claim 37 should be reversed for at least this additional reason.

I. Claim 38 and 39

Claims 38 and 39 depend from claim 25 and recite that the interconnect includes a compliant layer.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest the interconnect of claim 25, wherein the interconnect includes a compliant layer. The portion pointed to in the annotated Figure 13C of the Examiner and characterized by the Examiner as the "compliant layer" is not even asserted as being part of the alleged interconnect. Accordingly, the Examiner has failed to establish even a prima facie case of obviousness with regard to claims 37 and 38. Accordingly, the rejection of claims 37 and 38 should be reversed.

J. Claim 43

Claim 43 depend from claim 42 which recites that the substrate comprising second dense circuit device. Claim 43 further recites that the substrate (second dense circuit device) and the first dense circuit device are separated by a space having conductive vias enabling electrical communication between the second dense circuit device and the first dense circuit device.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest the method of claim 43 wherein the substrate (second dense circuit device) and the first dense circuit device are separated by a space having conductive via enabling electrical communication between the second dense circuit device and the first dense circuit device. In the annotated Figure 13C relied upon by the Examiner to reject claim 43, the Examiner points to a "spacer" and a "conductive via."

However, the " spacer" pointed to by the Examiner is actually a void or space between module 800 and circuit board 1300. As known to those ordinary skill in the art, a spacer is something that creates a space, not the void or space itself.

Moreover, the portion of the circuit board 1300 of Eichelberger characterized as the "conductive via" by the Examiner does not provide electrical communication between circuit board 1300 (characterized by the Examiner has the second dense

circuit device) and the top layers of model 800 (characterized by the Examiner as the first dense circuit device). In contrast, the "conductive via" pointed to by the Examiner merely extends through circuit board 1300. Accordingly, the rejection of claim 43 should be reversed for at least this additional reason.

K. Claim 44

Claim 44 recites a method which involves a dense circuit device, a spacer substrate and a clamping substrate. Claim 44 recites that they surface of the spacer substrate is covalently bonded to a surface of one of a dense circuit device or the clamping substrate. An interconnect is oriented between the dense circuit device and the clamping substrate. Another surface of the spacer substrate is then covalently bonded to a surface of the other of the dense circuit device and the clamping substrate to mechanically clamp the interconnect to the dense circuit device.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest the method of claim 44. It is clear that Eichelberger does not disclose a spacer substrate having one surface covalently bonded to a dense circuit device and another surface covalently bonded to a clamping substrate such that the clamping substrate and the dense circuit device mechanically clamp an interconnect therebetween. In fact, the Examiner's annotation of Figure 13B places the alleged spacer substrate completely out of contact with the alleged clamping substrate. The Examiner's "interconnect" spaces the clamping substrate from the alleged spacer substrate. Thus, the Examiner's own annotations do not even meet the limitations of claim 44.

Even assuming, arguendo, that it would be obvious to use so as to mechanically clamp an interconnect to a dense circuit device. as alleged to be taught by Tong in the arrangement of Eichelberger, this would merely result in module 1000 being covalently bonded to circuit board 1300. No suggestion exists for alternatively breaking up the unitary multilayer module 1000 into distinct components (a dense circuit device and an interconnect) and then covalently bonding the components together. Such a modification would clearly destroy the

intended functioning in principle of operation of Eichelberger. (See MPEP 2143.01). Accordingly, the rejection of claim 44 should be reversed. The rejection of claims 45-48 which depend from claim 44 should be reversed for at least the same reasons.

L. Claim 46

Claim 46 depend from claim 44 and recites that the dense circuit device comprises a dimension of less than or about 25 mm.

Neither Eichelberger nor Tong, alone or in combination, disclose or suggest a denser device and even mention of less than or about 25 mm. As before, the Examiner attempts to fill the clear inadequacy of Eichelberger end of Tong by making the assertion that because the drawings are "not to scale" this somehow discloses the claimed dimensional range. This clearly does not establish a prima facie case of obviousness. The Examiner has not met his burden. Accordingly, the rejection of claim 44 is improper and should be reversed.

M. Claim 48

Claim 48 depend from claim 47 and recites that the interconnect comprises two sets of wires.

Once again, electrically conductive layers of a unitary multilayer module are not wires. Accordingly, the rejection of claim 48 should be reversed.

Conclusion

In view of the foregoing, the Appellants submit that claims 1-7 and 15-17 are not properly rejected under 35 U.S.C. § 102(e)as being anticipated by U.S. Patent 6555908 (Eichelberger) and are therefore patentable **(2)** claim 8 is not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6555908 (Eichelberger) in view of Official Notice and is therefore patentable; and **(3)** claims 9, 12-14, 25-29, 31-39, 41-48 and 87 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over by U.S. Patent 6555908 (Eichelberger) in view of U.S. Patent 6962835 (Tong) and are therefore patentable.

Summary

For the foregoing, it is submitted that the Examiner's rejections are erroneous, and reversal of the rejections is respectfully requested.

Dated this 23rd day of June, 2009.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Original) A method comprising:

orienting an interconnect with respect to a dense circuit device;
pressing the interconnect to the dense circuit device using a substrate; and
bonding the substrate to the dense circuit device sufficient to maintain the interconnect against the dense circuit device,
wherein the act of pressing comprises mechanically clamping the interconnect between the dense circuit device and the substrate.

2. (Previously Presented) The method of claim 1, wherein the act of orienting the interconnect comprises fitting a negative in the interconnect over a projection on the dense circuit device such that the negative receives and at least partially surrounds the projection.

3. (Original) The method of claim 1, wherein the act of orienting comprises orienting wires of the interconnect with electrical bond pads of the dense circuit device.

4. (Original) The method of claim 3, wherein the wires and the electrical bond pads overlap and at the overlap have a breadth from tens of nanometers to tens of microns.

5. (Original) The method of claim 3, wherein the wires and the electrical bond pads overlap and at the overlap have a space from tens of nanometers to tens of microns.

6. (Original) The method of claim 3, wherein the wires and the electrical bond pads overlap and at the overlap have a breadth of less than one micron.

7. (Original) The method of claim 3, wherein the wires and the electrical bond pads overlap and at the overlap have a space of less than one micron.

8. (Original) The method of claim 3, wherein the wires comprise copper.

9. (Original) The method of claim 1, wherein the act of bonding comprises covalently bonding the dense circuit device to the substrate.

10. (Withdrawn) The method of claim 1, wherein the act of bonding comprises ionic bonding of the dense circuit device to the substrate.

11. (Withdrawn) The method of claim 1, wherein the act of bonding comprises bonding the dense circuit device to the substrate using an adhesive.

12. (Original) The method of claim 1, wherein the act of bonding is performed at low temperature.

13. (Original) The method of claim 12, wherein the low temperature comprises room temperature.

14. (Original) The method of claim 1, further comprising:

covalently bonding wires of the interconnect with electrical bond pads of the dense circuit device.

15. (Original) The method of claim 1, wherein the dense circuit device comprises a length or width of less than or about twenty-five millimeters.

16. (Original) The method of claim 1, wherein the dense circuit device and the interconnect have different coefficients of thermal expansion.

17. (Original) The method of claim 1, wherein the substrate comprises a second dense circuit device.

18. (Previously Presented) The method of claim 1, further comprising:

fixing a spacer substrate to one of the dense circuit device or the substrate, and wherein the act of bonding comprises bonding the spacer substrate to an other of the dense circuit device or the substrate to which the spacer substrate is not yet fixed.

19. (Original) The method of claim 18, wherein the act of bonding comprises covalent, low-temperature bonding.

20. (Withdrawn) The method of claim 18, wherein the act of bonding comprises bonding with an adhesive.

21. (Original) The method of claim 18, wherein the substrate comprises a second dense circuit device and the spacer substrate comprises conductive vias to allow electrical communication between the dense circuit device and the second dense circuit device.

25. (Original) A method comprising:

providing a dense circuit device having a first surface prepared for covalent bonding;
providing a substrate having a second surface prepared for covalent bonding;
orienting an interconnect between the dense circuit device and the substrate; and
mechanically clamping the interconnect between the dense circuit device and the substrate by covalently bonding the first surface to the second surface.

26. (Original) The method of claim 25, wherein the act of providing the dense surface device comprises preparing the first surface and the act of providing the substrate comprises preparing the second surface.

27. (Original) The method of claim 25, wherein the acts of providing the dense circuit device and providing the substrate comprise planarizing the first surface and the second surface.

28. (Previously Presented) The method of claim 25, wherein the dense circuit device comprises a projection comprising the first surface and the act of orienting comprises fitting a negative in the interconnect over the projection such that the negative receives and at least partially surrounds the projection.

29. (Previously Presented) The method of claim 25, wherein the substrate comprises a projection comprising the second surface and the act of orienting comprises fitting a negative in the interconnect over the projection such that the negative receives and at least partially surrounds the projection.

30. (Withdrawn) The method of claim 25, wherein the act of orienting comprises placing the interconnect between two or more guides.

31. (Original) The method of claim 25, wherein the act of orienting comprises orienting wires of the interconnect with electrical bond pads of the dense circuit device.

32. (Original) The method of claim 31, wherein the wires and the electrical bond pads overlap and at the overlap have a breadth from about tens of nanometers to tens of microns.

33. (Original) The method of claim 31, wherein the wires and the electrical bond pads overlap and at the overlap have a breadth of less than one micron.

34. (Original) The method of claim 25, wherein the act of orienting comprises stiffening the interconnect.

35. (Original) The method of claim 25, wherein the act of mechanically clamping is performed at low temperature.

36. (Original) The method of claim 35, wherein the low temperature comprises room temperature.

37. (Original) The method of claim 25, further comprising forming a compliant layer between the interconnect and the substrate.

38. (Original) The method of claim 25, wherein the interconnect includes wires and a compliant layer.

39. (Original) The method of claim 25, wherein the interconnect includes wires, a compliant layer, and a stiffening layer.

40. (Withdrawn) The method of claim 25, wherein the interconnect includes grouped wires and an insulative layer.

41. (Original) The method of claim 25, wherein the first surface and the second surface comprise a silicon-containing material.

42. (Original) The method of claim 25, wherein the substrate comprises a second dense circuit device.

43. (Original) The method of claim 42, wherein the substrate and the first dense circuit device are separated by a spacer having conductive vias enabling electrical communication between the second dense circuit device and the first dense circuit device.

44. (Previously Presented) A method comprising:

planarizing a first surface of a dense circuit device;

planarizing a second surface of a spacer substrate;

planarizing a third surface of the spacer substrate;

planarizing a fourth surface of a clamping substrate;

covalently bonding one of the (a) first surface to the second surface or (b) the third surface to the fourth surface;

orienting an interconnect between the dense circuit device and the clamping substrate; and

mechanically clamping the interconnect to the dense circuit device by covalently bonding an other of the (a) first surface to the second surface or (b) the third surface to the fourth surface.

45. (Original) The method of claim 44, wherein the act of mechanically clamping is performed at low temperature.

46. (Original) The method of claim 44, wherein the dense circuit device comprises a dimension of less than or about twenty-five millimeters.

47. (Original) The method of claim 44, wherein the clamping substrate comprises a second dense circuit device.

48. (Original) The method of claim 47, wherein the interconnect comprises two sets of wires, the first set contacting the first dense circuit device and the second set contacting the second dense circuit device.

87. (Previously Presented) The method of claim 25 further comprising:preparing the first surface for covalent bonding and preparing the second surface for covalent bonding.

88. (Previously Presented) The method of claim 87, wherein the dense circuit device has a projection including the first surface and wherein the interconnect has a hole form by the second surface and wherein orienting the interconnect between the dense circuit device and the substrate includes orienting the projection in the hole.

89. (Previously Presented) The method of claim 88, wherein the hole is generally a negative of the projection.

90. (Previously Presented) The method of claim 88, wherein the act of orienting comprises orienting electrical bond pads of the dense circuit device with wires of the interconnect.

91. (Previously Presented) The method of claim 90, wherein the dense circuit device has a length or width of less than or about twenty-five millimeters and the electrical bond pads or the wires are less than one micron in breadth.

92. (Previously Presented) The method of claim 90, wherein the dense circuit device has a length or width of less than or about five millimeters and the electrical bond pads or the wires are less than or about ten microns in breadth.

93. (Previously Presented) The method of claim 90, wherein the act of covalently bonding mechanically bonds wires of the interconnect with electrical bond pads of the dense circuit device.

EVIDENCE APPENDIX

There is no evidence previously submitted under 37 C.F.R. §§ 1.130, 1.131 or 1.132 or other evidence entered by the Examiner and relied upon by Appellant in this appeal. Accordingly, the requirements of 37 C.F.R. §§ 41.37(c)(1)(ix) are satisfied.

RELATED PROCEEDINGS APPENDIX

There are no decisions rendered by a Court of the Board in a proceeding identified in the Related Appeals and Interferences section. Accordingly, the requirements of 37 C.F.R. §§ 41.37(c)(1)(x) are satisfied.